This paper must not be removed from the examination room

STUDENT NAME: _____

STUDENT NO.: _____

THE UNIVERSITY OF QUEENSLAND

School of Information Technology & Electrical Engineering

<Second Semester Degree Examination, November 2005>

CSSE4000 / 7101

Digital System Design II

TIME: **TWO** hours for working

15 minutes for perusal before examination begins

ANSWER ALL QUESTIONS ON ANSWER BOOKLET PROVIDED

CLOSED BOOK EXAMINATION

Drawing instruments and one electronic calculator may be used but NO pre-programmed material or calculator instruction booklets are allowed in the examination room. No printed or hand-written material is allowed.

CSSE4000/7101 Digital System Design II
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Question 1 (40 marks) – design combinational logic

1. Present a circuit diagram of 3 input NAND static CMOS gate. Resize the transistors to achieve symmetrical output. (5 marks)

2. Calculate internal capacitances of this gate. Show the capacitances on the circuit diagram of the gate. (10 marks)

3. The resized gate is driving 2 standard loads (2 min size inverters). Calculate accurately rise and fall delays of that gate. (15 marks)
   HINT: Take into account all capacitances that need to be charged/discharged

4. Present a circuit diagram of 3 input AND dynamic (domino logic) CMOS gate.
   Describe operation, define rise and fall times.
   Show/comment on how to calculate rise and fall times accurately.
   (10 marks)

The minimum size MOS transistor parameters :

NMOS equivalent on-resistance $R_n = 11\ k\Omega$
PMOS equivalent on-resistance $R_p = 33\ k\Omega$
Gate capacitance $C_g = 0.7\ fF$
Gate drain/source capacitance $C_{gd} = C_{gs} = 0.2\ fF$
Drain/source bulk capacitance $C_{db} = C_{sb} = 0.7\ fF$

Question 2 (30 marks) – miscellaneous

1. Explain the relation between fan-in, fan-out and the delay of static CMOS gate. (5 marks)
2. Analyse properties of PMOS and NMOS transistors as electrical switches. (7 marks)
   Hint: Why PMOS is used for Pull Up and NMOS for Pull Down ?

3. Draw the schematic of a transmission gate. Explain why it has better properties as a switch than a single MOS transistor (3 marks)

4. Explain and discuss the dynamic, direct-path (short circuit) and static power consumption in static CMOS. (15 marks)

Question 3 (25 marks) – sequential logic

a) Draw the schematics of a static, inverter/multiplexer based latch. (5 marks)
(Hint: use switches to implement the multiplexer)

b) Show calculations of T_{setup}, T_{hold} and T_{delay} for the latch in question a. (7 marks)

c) Explain constraints on the clock in latch based sequential logic design (6 marks)

d) Define and explain two phase clocking system. Explain how the single clock constraints are alleviated. (7 marks)

Question 4 (25 marks) – system

a) Explain problems with clock and power distribution on CMOS chip and present most popular solutions
(10 marks)

b) Explain problems and advantages of synchronous systems, discuss alternatives
(7 marks)

c) Explain essential differences between full custom, standard cell, gate array and field programmable logic technologies (8 marks)

 END