

IDE

SIFA Storage

Rational Rose

Draft Domain

DTD to Rose

Eclipse Modelling Framework (EMF)Domain
Structure

Rose to Ecore

Ecore to OZ

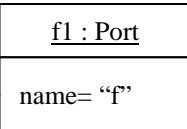
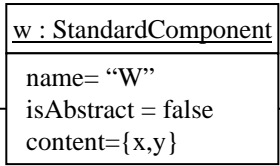
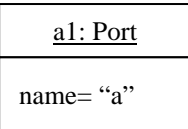
Formalized
Domain

OZ to OZ

Community Z Tools (CZT)Type Error
Report

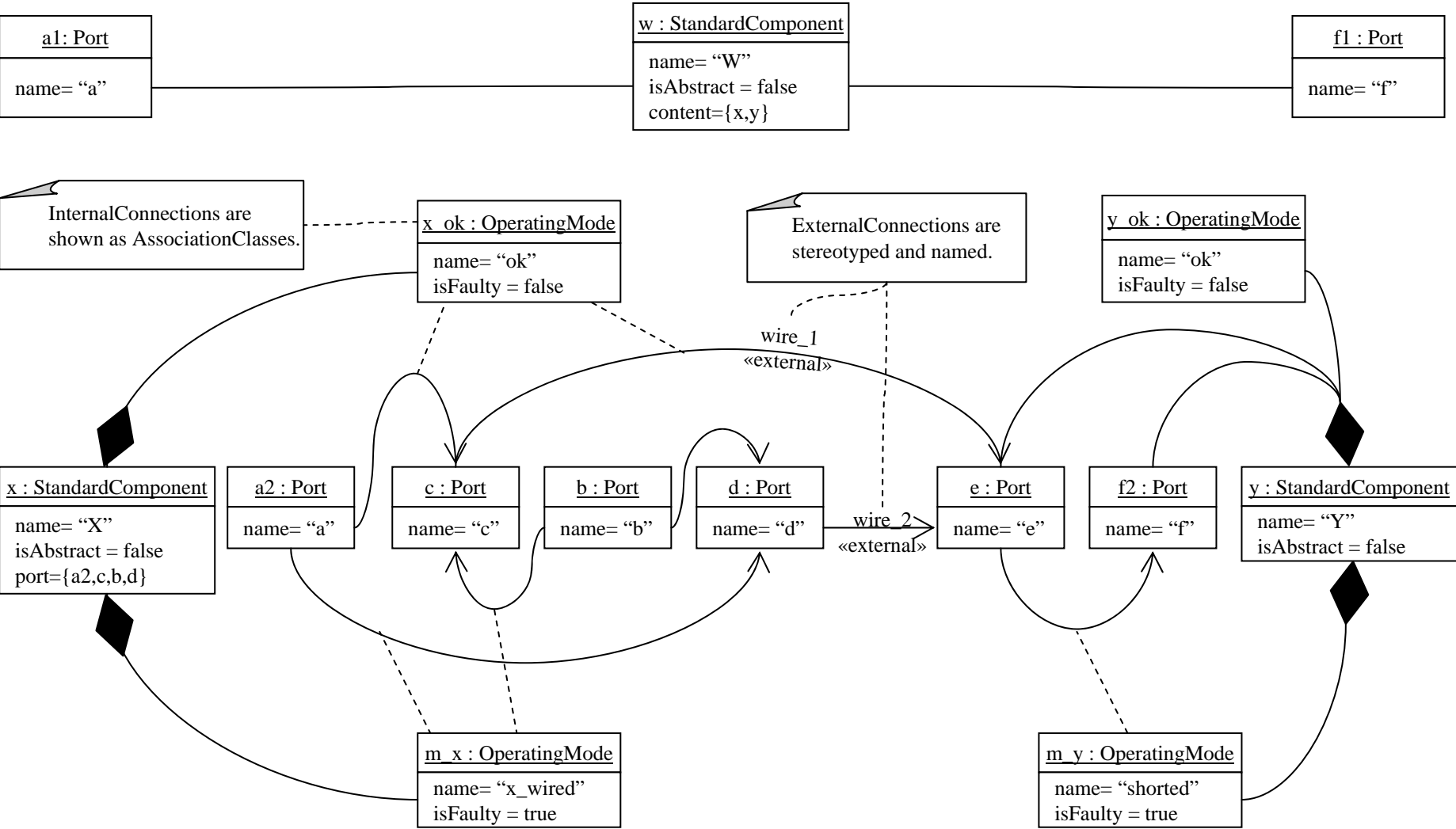
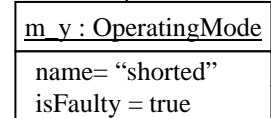
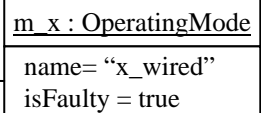
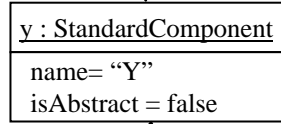
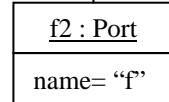
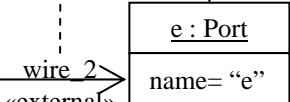
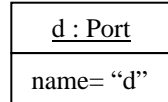
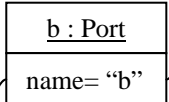
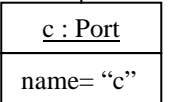
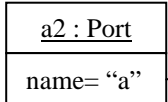
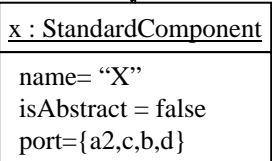
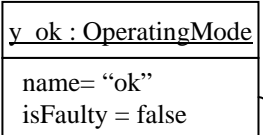
Type Checker

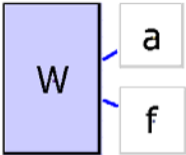
Formalized
Domain



InternalConnections are shown as AssociationClasses.

ExternalConnections are stereotyped and named.



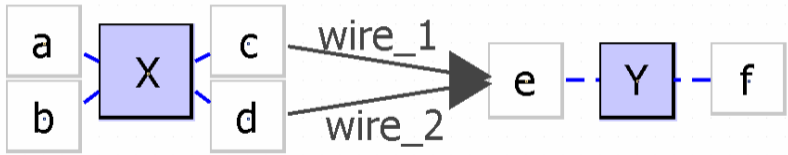


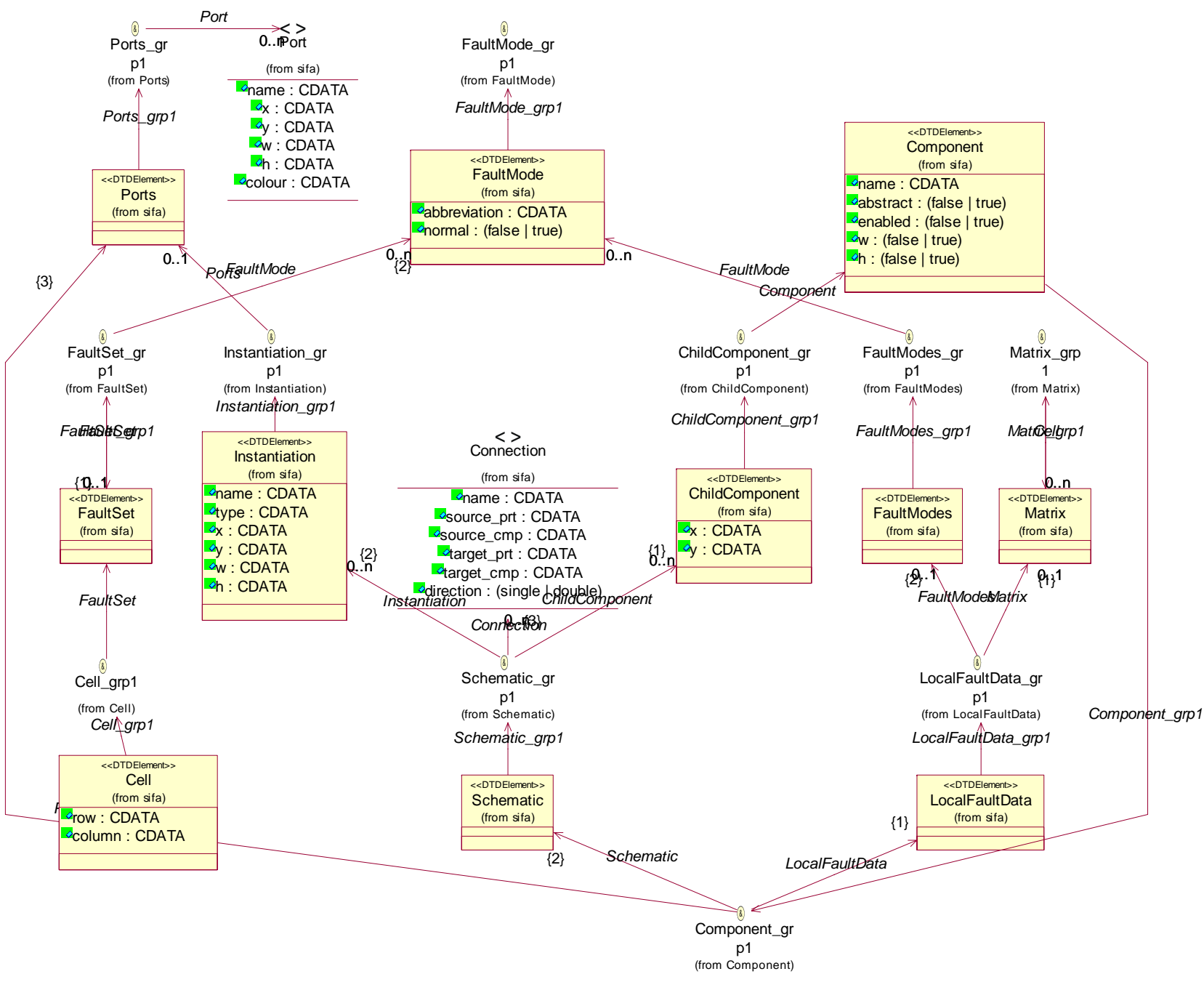
Internal connections:

Y	e	f
e	shorted	
f		ok

X	a	b	c	d
a	ok		ok	x_wired
b		ok	x_wired	ok
c			ok	
d				ok

contains:





- + NMC27C16B
- Cap
- Cap_Pol1
- Header_2
- IQXPMINUS350
- LED1
- + PIC16F877
- Res1
- + ST232
- SWMINUSSPDT
- XTAL
- Generic Dual-Int
- Generic Oct-Int
- Generic Single-Int
- J-K-CLK-CLR-F
- Generic Dual JK
- 3-8 Decoder La
- Generic 3-8 De
- + M74HC14B1R
- 2-ch Multiplexe
- + Generic Quad 2
- 4-bit counter
- 8-bit EPROM
- 8-bit CMOS Fla
- Generic RS232
- Generic RS232
- + Comparison_Logic
- Dict_addressing
- Library
- + DA_Architecture
- + PICS_and_CLK
- Top Level Connecti
- DA_Sheet

3 Gate

Component Analysis

Schematic Matrix

[COMPONEN...	in1	in0	out	in2
in1	{{3 Gate[no...	<input type="checkbox"/>	{{3 Gate[normal]}}	<input type="checkbox"/>
in0	<input type="checkbox"/>	{{3 Gate[normal],...	{{3 Gate[normal]}}	<input type="checkbox"/>
out	<input type="checkbox"/>	<input type="checkbox"/>	{{3 Gate[normal]}, {3 Gate[fault]}	<input type="checkbox"/>
in2	<input type="checkbox"/>	<input type="checkbox"/>	{{3 Gate[normal]}}	{{3 Gate[normal]}, {3 Gate[fault]}}

Operation Modes

- normal : normal
- fault : fault

Abbreviation:

Description:

